

526 Rec'd PCT/PTO 05 JAN 2001  
09/743143

CERTIFICATION UNDER 37 CFR 1.10

I hereby certify that this Transmittal Letter and the papers indicated as being transmitted therewith are being deposited with the United States Postal Service on this date shown below in an envelope as "Express Mail Post Office to Addressee" under the below indicated Mailing Label Number, addressed to: Box PCT, Assistant Commissioner for Patents, Washington, D.C. 20231.

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ATTORNEY'S DOCKET NO. YAMAP0749US

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
(DO/EO/US)**

In re national phase of:

Applicant(s): Eiji Miyagoshi  
International Application No.: PCT/JP99/03766  
International Filing Date: 13 July 1999  
Priority Date Claimed: 15 July 1998  
Title of Invention: DECODING DEVICE AND DECODING METHOD

**TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED  
OFFICE (DO/EO/US) CONCERNING ENTRY INTO U.S. NATIONAL  
PHASE UNDER 35 U.S.C. 371**

Box PCT  
Assistant Commissioner for Patents  
Washington D.C. 20231

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information under 35 U.S.C. 371:

1. This express request to immediately begin national examination procedures (35 U.S.C. 371(f)).
2. The U.S. National Fee (35 U.S.C. 371(c)(1)) and other fees (37 CFR 1.492) as indicated below.

3. A copy of the International application (35 U.S.C. 371(c)(2)):
- ☒ is transmitted herewith  
(International Publication No. \_\_\_\_\_).
  - ☐ is not required, as the application was filed with the United States Receiving Office.
  - ☐ has been transmitted by the International Bureau. A copy of Form PCT/IB/308 is enclosed.
4. ☐ A translation of the International application into the English language (35 U.S.C. 371(c)(2)) is transmitted herewith.
5. Amendments to the claims of the International application under PCT Article 19 (35 U.S.C. 371(c)(3)):
- ☐ are transmitted herewith.
  - ☐ have been transmitted by the International Bureau.
6. ☐ A translation of the amendments to the claims under PCT Article 19 (38 U.S.C. 371(c)(3)) is transmitted herewith.
7. A copy of the international examination report (PCT/IPEA/409)
- ☐ is transmitted herewith.
  - ☐ is not required as the United States Patent and Trademark Office was the IPEA.
8. Annex(es) to the international preliminary examination report
- ☐ is/are transmitted herewith.
  - ☐ is not required as the United States Patent and Trademark Office was the IPEA.
9. ☐ A translation of the annexes to the international preliminary examination report is transmitted herewith.

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10. ☐ An oath or declaration of the inventor (35 U.S.C. 371(c)(4)) complying with 35 U.S.C. 115 is submitted herewith.
11. An International Search Report (PCT/ISA/210)
- a. ☐ is transmitted herewith.
- b. ☐ has been transmitted by the International Bureau.
- c. ☐ is not required, as the application was searched by the United States International Searching Authority.
12. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98 is transmitted herewith, along with Form PTO-1449 and copies of citations listed.
13. ☐ An assignment document is transmitted herewith for recording, along with a separate cover sheet.
14. ☐ A preliminary amendment is enclosed.
15. ☐ A verified statement claiming small entity status is enclosed.
16. ☐ Other:

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Basic National Fee					Fee
IPEA - US					\$690.00
ISA - US					\$710.00
PTO not ISA or IPEA					\$1,000.00
Claims meet PCT Art. 33(1)-(4) - IPEA - US					\$100.00
Filing with EPO or JPO search report					\$860.00
Enter appropriate basic fee →					\$860.00
Claims*	Number filed		Number extra	Rate	
Total claims	5	-20	0	\$18.00	\$0.00
Independent claims	2	-3	0	\$80.00	\$0.00
Multiple dependent claims (if applicable)				\$270.00	
Total of above					\$860.00
Small entity statement enclosed, 1 if Yes, 0 if No →				0	\$0.00
Total national fee					\$860.00
Fee for recording enclosed assignment				\$40.00	
Total fees enclosed					\$860.00

\*After any attached preliminary amendment reducing the number of claims and/or deleting multiple dependencies.

☒ [X] A check in the amount of \$ 860.00 to cover the above fees is enclosed.

☐ [ ] Please charge our Deposit Account No. 18-0988 in the amount of \$          . A duplicate copy of this sheet is enclosed.

WARNING: TO AVOID ABANDONMENT OF THE APPLICATION THE BASIC NATIONAL FEE MUST BE PAID WITHIN THE 20/30 MONTH TIME LIMIT.

16. The Commissioner is hereby authorized to charge the following additional fees that may be required by this paper and during the entire pendency of this application to our Deposit Account No. 18-0988:

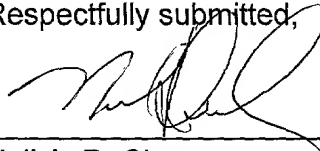
a. ☒ 37 CFR 1.492(a)(1), (2), (3), (4) and (5) (filing fees)

WARNING: BECAUSE FAILURE TO PAY THE NATIONAL FEE WITHIN 30 MONTHS WITHOUT EXTENSION (37 CFR S 1.495(B)(2)) RESULTS IN ABANDONMENT OF THE APPLICATION, IT WOULD BE BEST TO ALWAYS CHECK THE ABOVE BOX.

b. ☐ 37 CFR 1.492(b), (c) and (d) (presentation of extra claims)

NOTE: Because additional fees for excess or multiple dependent claims not paid on filing or on later presentation must only be paid or these claims cancelled by amendment prior to the expiration of the time period set for response by the PTO in any notice of fee deficiency (37 CFR 1.492(d)), it might be best not to authorize the PTO to charge additional claim fees, except possibly when dealing with amendments after final action.

Respectfully submitted,



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426 Rec'd PCT/PTO 05 JAN 2001  
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- 1 -

## DESCRIPTION

### DECODING DEVICE AND DECODING METHOD

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#### TECHNICAL FIELD

The present invention relates to a decoding device and a decoding method for decoding a bit stream including a plurality of packets.

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#### BACKGROUND ART

A decoding device for decoding a bit stream including a plurality of packets is known. Each of the plurality of packets includes a header portion and a data portion. A picture start code indicating a leading position of an access unit is located at an arbitrary position in the data portion.

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A skip reproduction operation and a freeze reproduction operation are known as special reproduction operations of video data and audio data. A skip reproduction operation is implemented by skipping at least one of a plurality of access units. A freeze reproduction operation is implemented by repeatedly reproducing at least one of the plurality of access units.

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It is necessary to specify the leading position of the access unit for implementing the skip reproduction operation. For this purpose, the conventional decoding device is required to detect the picture start code included in the data portion of a packet by searching the data portion of the packet. However, searching the data portion of the

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packet is time-consuming. Therefore, it is difficult to perform the skip reproduction operation smoothly.

5 The conventional decoding device performs the freeze reproduction operation by accumulating the bit stream to a buffer memory first and then repeatedly reading specific data included in the bit stream which is accumulated in the buffer memory. Therefore, the conventional decoding device needs a large capacity buffer memory for display.

10 The present invention has objectives of: (1) providing a decoding device and a decoding method implementing a fast skip reproduction operation; and (2) providing a decoding device and a decoding method which  
15 eliminates the necessity of a buffer memory for display.

#### DISCLOSURE OF THE INVENTION

20 A decoding device according to the present invention is a decoding device for decoding a bit stream including a plurality of packets, in which data corresponding to an access unit includes a first data portion and a second data portion, the decoding device including: a packet regeneration section for receiving a first packet and a  
25 second packet following the first packet, and when the first packet includes the first data portion and the second packet includes the second data portion, producing a new packet including the data corresponding to the access unit by combining the first data portion and the second data portion;  
30 and a decoding section for decoding the data corresponding to the access unit, wherein the new packet includes information indicating a length of the data corresponding to the access unit. Thus, the above-described objectives

are achieved.

The new packet may further include information indicating a presentation time stamp.

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The packet regeneration section may generate a plurality of new packets, and the decoding device may further include a storage section for storing the plurality of new packets generated by the packet regeneration section; and  
10 a read control section for controlling a reading operation of the plurality of new packets from the storage section so as to skip at least one of the plurality of new packets by using the information indicating the length of the data corresponding to the access unit.

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The packet regeneration section may generate a plurality of new packets, and the decoding device may further includes a storage section for storing the plurality of new packets generated by the packet regeneration section; and  
20 a read control section for controlling a reading operation of the plurality of new packets from the storage section so as to repeatedly read at least one of the plurality of new packets by using the information indicating the length of the data corresponding to the access unit.

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A decoding method according to the present invention is a decoding method for decoding a bit stream including a plurality of packets, in which data corresponding to an access unit includes a first data portion and a second data  
30 portion, the decoding method including the steps of: receiving a first packet and a second packet following the first packet, and when the first packet includes the first data portion and the second packet includes the second data



portion, producing a new packet including the data corresponding to the access unit by combining the first data portion and the second data portion; and decoding the data corresponding to the access unit, wherein the new packet includes information indicating a length of the data corresponding to the access unit. Thus, the above-described objectives are achieved.

#### BRIEF DESCRIPTION OF THE DRAWINGS

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Figure 1 illustrates an exemplary structure of a DVD reproduction apparatus 300 including a decoding device 1 according to the present invention.

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Figure 2A schematically illustrates a structure of a bit stream 100.

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Figure 2B is a diagram showing how a PES packet 164 is generated.

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Figure 3 illustrates a structure of the decoding device 1 according to an embodiment of the present invention.

Figure 4 illustrates a structure of a packet regeneration section 10.

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Figure 5 illustrates a structure of a read control section 30.

Figure 6A illustrates an example of a syntax and a bit array of a pack header 120.

Figure 6B illustrates an example of a syntax and a bit array of a PES header 140.

5 Figure 7 illustrates an example of a bit stream 160 including PES packets 164a-164d generated by a PES packet generation section 54.

#### BEST MODE FOR CARRYING OUT THE INVENTION

10 Hereinafter, examples of the present invention will be described with reference to the figures.

15 Figure 1 shows an exemplary structure of a DVD reproduction apparatus 300 including a decoding device 1 according to the present invention.

The DVD reproduction apparatus 300 includes a pickup unit 320, a physical block 330, the decoding device 1, an output device 350, a CPU 360, and an input device 370.

20 A DVD 310 has video data and audio data recorded thereon. The data recorded on the DVD 310 is read and reproduced by the DVD reproduction apparatus 300. The disk 310 is described as a DVD in this specification, but can be any other information recording medium.

30 The pickup unit 320 reads data recorded on the DVD 310. Data is read by irradiating the DVD 310 with laser light having a prescribed wavelength from a laser unit 321 and detecting the laser light reflected by the DVD 310. The pickup unit 320 outputs the read data to the physical block 330.

The physical block 330 includes an error code correction unit 331 and a servo control unit 332. The physical block 330 receives data output from the pickup unit 320. The received data is subjected to signal processing, such as, for example, error code correction by the error code correction unit 331. The physical block 330 outputs the processed data to the decoding device 1 as a bit stream 100.

The decoding device 1 receives the bit stream 100 which has been output from the physical block 330. The decoding device 1 receives a control signal 361 which indicates a reproduction operating mode from the central processing unit (CPU) 360. The decoding device 1 carries out a decoding process of the bit stream 100 according to the reproduction operating mode indicated by the control signal 361. The decoding device 1 outputs a video signal 200a and/or an audio signal 200b to the output device 350 as a decoded result of the bit stream 100.

Details of a structure and operation of the decoding device 1 will be described later.

The output device 350 displays the video signal 200a which has been output from the decoding device 1 on a display, such as, a television for example, and outputs the audio signal 200b which has been output from the decoding device 1 to a speaker. The data is thus output from the decoding device 1 in a format in which the data can be output to the display or the speaker.

The central processing unit (CPU) 360 controls the pickup unit 320, the physical block 330, the decoding

device 1, and the output device 350. When a command indicating the reproduction operating mode (e.g., normal reproduction mode, double speed reproduction mode, freeze reproduction mode) is input from the input device 370, the CPU 360 generates the control signal 361 corresponding to the command and outputs the control signal 361 to the decoding device 1.

The input device 370 is used for allowing a user to input the command indicating the reproduction operating mode. Such a command is input by using, for example, a remote controller (not shown) or an operation panel (not shown) provided in the DVD reproduction apparatus 300.

In the example described above, it is assumed that the bit stream 100 to be input to the decoding device 1 is data which has been read from the DVD 310 and has been processed. However, the bit stream data 100 can be data obtained from an accumulation medium or a broadcasting medium. Herein, an accumulation medium can be, for example, a CD-ROM, an LD, or a video tape, and a broadcasting medium can be, for example, television broadcasting, satellite broadcasting, or data communication.

Hereinafter, a structure of the bit stream 100 to be input to the decoding device 1 will be described.

Figure 2A schematically illustrates the structure of the bit stream 100.

The bit stream 100 illustrated in Figure 2A is in conformity with the MPEG2 standard. However, the bit stream 100 to be input to the decoding device 1 is not

limited to a stream in conformity with the MPEG2 standard. Any bit stream which includes data corresponding to an access unit described below can be input to the decoding device 1.

5           The bit stream 100 includes at least one pack 110. The pack 110 includes a pack header 120 and at least one packet 130. The packet 130 includes a PES header 140 and a data portion 150.

10           In the data portion 150, either video data 150a or audio data 150b is stored. In a DVD, a data length of the data portion 150 is fixed. However, in an MPEG data stream, a data length of the data portion 150 does not need to be a fixed length.

15           The video data 150a includes not only data of a main video but also data of a sub-video. Herein, main video refers to major video included in movies or television broadcasting, and sub-video refers to video representing  
20 additional information to the main video data, such as language subtitles or a title.

          The audio data 150b corresponds to the video represented by the video data 150a, or is independent from  
25 the video represented by the video data 150a.

          As shown in Figure 2A, a picture start code 162a defines a boundary between an access unit and the next access unit (an access unit boundary 163a). Herein, the term  
30 "access unit" is defined as a smallest data unit which can be individually decoded. In the case of the video data 150a, an access unit can be one field or one frame.

5 Data corresponding to one access unit is not necessarily included in the data portion 150 of one packet 130. For example, as shown in Figure 2A, there is a case where a portion of video data 150a corresponding to one access unit (a first data portion 150a-1) is included in a data portion 150 of a packet 130, and another portion of the video data 150a corresponding to the same access unit (a second data portion 150a-2) is included in a data portion 150 of another packet 130. In this case, the decoding device 1 according to the present invention generates video data 150A by combining the first data portion 150a-1 and the second data portion 150a-2, and generates a new packet 164 by combining the video data 150A and a PES header 141 (see Figure 2B). The new packet 164 is thus generated to include data corresponding to one access unit.

20 In the case where data corresponding to one access unit is distributed in three or more packets, a new packet 164 is generated to include data corresponding to one access unit by combining data in these packets.

25 Alternatively, there may be a case where data corresponding to a plurality of access units are included in a data portion 150 of one packet 130. In this case, the decoding device 1 according to the present invention divides the data of the data portion 150 to correspond to the plurality of access units. Therefore, a plurality of new packets 164 are generated so that each packet includes data corresponding to one access unit.

30 Figure 6A illustrates an example of a syntax and a bit array of the pack header 120.

The pack header 120 is identified by a value of pack\_start\_code. When the value of pack\_start\_code is 000001BA (hexadecimal), it is detected that the pack header 120 is in the bit stream 100. A typical example of the information provided in the pack header 120 is a system\_clock\_reference (SCR). An SCR is information indicating a reference time of a presentation timing of the video data 150a or the audio data 150b.

Figure 6B illustrates an example of a syntax and a bit array of the PES header 140.

The PES header 140 is identified by a value of packet\_start\_code\_prefix and a value of stream\_id.

A field indicating packet\_length and a field indicating packet\_data\_byte are provided in the PES header 140.

The packet\_length field defines the number of bytes in the PES header 140 of this field and subsequent fields.

Information indicating a presentation time stamp (PTS) or the like may additionally be provided between the packet\_length field and the packet\_data\_byte field. A PTS is information indicating a relative display time with respect to the reference time indicated by the SCR.

The packet\_data\_byte field represents the video data 150a or the audio data 150b. When the value of the stream\_id is EX (hexadecimal; X is arbitrary), the packet\_data\_byte field represents the video data 150a.

Herein, the number of the bytes in the packet\_length field and between the packet\_length field and the packet\_data\_byte field is predetermined by the syntax to be a fixed number of bytes. Thus, the value obtained by subtracting this fixed number of bytes from the number of bytes indicated by packet\_length is equal to the number of bytes of the packet\_data\_byte. The length of the video data 150a or the audio data 150b can be calculated by calculation based on packet\_length. This enables extraction of the video data 150a or the audio data 150b from the bit stream 100.

Figure 3 illustrates a structure of the decoding device 1 according to an embodiment of the present invention.

The decoding device 1 includes a packet regeneration section 10, a data storage section 20, a read control section 30, a decoding section 40, and an input section 50.

The packet regeneration section 10 receives the bit stream 100 and generates a bit stream 160 which is packed in access units. The generated bit stream 160 is output to the data storage section 20. A detailed structure and operation of the packet regeneration section 10 will be described later with reference to Figure 4.

The data storage section 20 receives the bit stream 160 which is packed in access units from the packet regeneration section 10 and temporarily stores the received bit stream 160. The data storage section 20 also receives a read address signal 550, which indicates the location of



the stored bit stream 160 which is packed in access units, from the read control section 30. The data storage section 20 reads the bit stream 160 from the location of the storage area corresponding to the address represented by the received read address signal 550, and outputs the read bit stream 160 to the read control section 30 as a data signal 560.

The data storage section 20 can be, for example, a DRAM.

The read control section 30 receives a control signal 362 which has been output from the input section 50. The control signal 362 is a signal indicating a reproduction operating mode of the bit stream 100. The read control section 30 generates the address signal 550 according to the reproduction operating mode indicated by the control signal 362, and outputs the generated address signal 550 to the data storage section 20. The read control section 30 receives the data signal 560 which has been output from the data storage section 20, and outputs the received data signal 560 to the decoding section 40 as a data signal 561. A detailed structure and operation of the read control section 30 will be described later with reference to Figure 5.

The decoding section 40 receives the data signal 561 from the read control section 30, and decodes the received data signal 561. The decoding section 40 outputs the video signal 200a and/or the audio signal 200b which has been decoded from the data signal 561 to the output device 350 outside the decoding device 1.

Hereinafter, a structure and operation of the packet regeneration section 10 included in the decoding device 1 will be described.

5           Figure 4 illustrates the structure of the packet regeneration section 10.

          The packet regeneration section 10 includes a start  
code detector 51, a divider 52, a PES header storage  
10       section 53, and a PES packet generation section 54.

          The start code detector 51 receives the bit  
stream 100 and detects a start code. The start code is a  
code inserted into a leading position of the pack header 120,  
15       a leading position of the PES header 140, and a leading  
position of an access unit 151a included in the bit  
stream 100. For example, the start code is a bit string of  
24 bits, such as "0000 0000 0000 0000 0000 0001". The start  
code detector 51 outputs the received bit stream 100 to the  
20       divider 52. When the start code appears in the input bit  
stream 100, the start code detector 51 outputs a start code  
detection signal to the divider 52.

          The divider 52 receives the bit stream 100 and the  
25       start code detection signal from the start code detector 51.

          When the divider 52 receives the start code  
detection signal, the divider 52 reads data of a  
predetermined number of bits (for example, 8 bits) following  
30       the start code, and examines whether the data matches a  
predetermined bit string. As a result, the divider 52  
determines the kind of data corresponding to the start code.

For example, when the 8 bits following the start code match "1110 XXXX", the divider 52 determines that the data is the PES header 140 corresponding to the video data 150a. When the 8 bits following the start code are "1100 XXXX", the divider 52 determines that the data is the PES header 140 corresponding to the audio data 150b. A synchronous word which is referred to as Sync byte may be used for determining the boundary between the access units in the audio data 150b. In this case, the device may be arranged so that the synchronous word is detected in the start code detector 51.

When the divider 52 detects the PES header 140 in the bit stream 100, the divider 52 outputs a PES header detection signal to the PES header storage section 53. Thus, the PES header 140 extracted from the bit stream 100 is stored in the PES header storage section 53.

The syntax of the pack header 120 and the PES header 140 are as illustrated in Figures 6A and 6B respectively. According to the respective syntax, the pack header 120 and the PES header 140 are extracted from the bit stream 100.

Hereinafter, an example in which the video data 150a is stored in the data portion 150 of the packet 130 will be described. However, this is merely an example, and the data to which the present invention is applicable is not limited to the video data 150a. The present invention can be applied to any data which can become a target of a special reproduction. For example, the video data 150a, the audio data 150b, and other kinds of data can be a target of the special reproduction.

When the video data 150a following the PES header 140 is input to the start code detector 51, the start code detector 51 detects the start code. For example, in the case where the 8 bits following the start code are "0000 0000", the divider 52 determines that the data is the picture start code 162a, and outputs a picture start code detection signal to the PES packet generation section 54.

The PES header storage section 53 stores the PES header 140 extracted from the bit stream 100 by the divider 52. A PES header detection signal from the divider 52 is used as an enable signal which permits the storage of the PES header 140 in the PES header storage section 53.

The PES header storage section 53 may alternatively store only a portion of the data of the PES header 140 (for example, packet\_length, or packet\_length and PTS) instead of storing the entire data of the PES header 140.

The PES packet generation section 54 receives the picture start code detection signal from the divider 52. A counter 54a initializes a count value in response to the picture start code detection signal. The count value represents the number of bytes of the video data 150a which are input to the counter 54a from the point of receiving a certain picture start code detection signal to the point of receiving the next picture start code detection signal. Thus, the counter 54a is used for counting the number of bytes from the leading position of an access unit to the leading position of the next access unit (i.e. a length of the access unit).

5 The PES packet generation section 54 additionally receives the PES header 140 stored in the PES header storage section 53. The PES header 140 is stored in a packet length update section 54b. In the packet length update section 54b, the value of packet\_length of the PES header 140 is updated so as to match the length of the access unit counted by the counter 54a. The packet length update section 54b outputs the PES header 140 which has the updated packet\_length to a combining section 54d as the PES header 141.

15 The PES packet generation section 54 additionally receives the video data 150a which starts from the picture start code 162a. The video data 150a is stored in the buffer 54c. Herein, as shown in Figure 2B, when a portion of the video data 150a (a first data portion 150a-1) is included in the data portion 150 of a first packet 130 and another portion of the video data 150a (a second data portion 150a-2) is included in the data portion 150 of a second packet 130 following the first packet, the first data portion 150a-1 and the second data portion 150a-2 are stored in the buffer 54c, and the first data portion 150a-1 and the second data portion 150a-2 are combined together in the buffer 54c. As a result, the video data 150A corresponding to one access unit 151a is output from the buffer 54c to the combining section 54d.

30 The combining section 54d receives the PES header 141 from the packet length update section 54b, receives the video data 150A corresponding to the access unit 151a from the buffer 54d, and combines the PES header 141 and the video data 150A. Thus, a new PES packet 164 including the video data 150A corresponding to

the access unit 151a is generated. The PES packet 164 is output to the data storage section 20.

5        Herein, the PES header 141 which is to be combined to the video data 150A corresponding to the access unit 151a is obtained by updating packet\_length of the last one of a plurality of PES headers 140 which appeared prior to the first data portion 150a-1 including the picture start code 162a.

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      The information included in the PES header 141 can be same as the information included in the PES header 140. However, it is sufficient that the PES header 141 includes a portion of the information included in the PES header 140 because the PES header 140 includes information not necessarily needed for the PES header 141.

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      For example, from a viewpoint of implementing a special reproduction operation, it is enough for the PES header 141 to include the packet\_length. This is because, with reference to the packet\_length value in the PES header 141, the data length of the access unit 151a including the picture start code 162a can be obtained, and the special reproduction operation can be performed by using this data length. Such a process is executed by the read control section 30 which will be described later. Moreover, it is preferable that the PES header 141 further includes pack\_start\_code\_prefix, stream\_id and the PTS. Alternatively, the PTS can be inserted into a predetermined position of the video data 150A.

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      The packet length update section 54b can be structured to select information which is needed for the

PES header 141 from the information included in the PES header 140, and to output the PES header 141 including the selected information. The information selected by the packet length update section 54b can be predetermined information included in the PES header 140, or can be information selected according to the data following the PES header 140 in the information included in the PES header 140.

By repeating the operation described above, the PES packet generation section 54 generates a plurality of new PES packets 164. Each of the plurality of PES packets 164 includes video data corresponding to one access unit.

Figure 7 illustrates an example of the bit stream 160 including PES packets 164a-164d generated by the PES packet generation section 54.

The PES packet generation section 54 can generate the PES packet 164 including audio data corresponding to one access unit, similar to the case of video data described above.

Addition of other information to the PES header 140 will not be a problem even though it is out of the range of the MPEG2 system stream standard, if there are appropriate guidelines related to the handling of the other information between the decoding section 40 and the PES header 140.

Hereinafter, a structure and operation of the read control section 30 included in the decoding device 1 will be described.

Figure 5 illustrates the structure of the read control section 30.

5 The read control section 30 includes a controller 500, address generators 501a and 501b, an address selection circuit 502, and FIFO (first-in first-out) memories 503a and 503b.

10 A control signal 362 indicating a reproduction operating mode is input to the controller 500. The controller 500 controls a reproduction of the bit stream 100 according to the control signal 362. The operation of the read control section 30 when the reproduction operating mode is a normal reproduction mode, and the operation of the read  
15 control section 30 when the reproduction operating mode is a double speed reproduction mode or a freeze reproduction mode will be described later.

20 When the reproduction operating mode is the normal reproduction mode, the controller 500 sets a read address 506a in the address generator 501a and outputs a read starting signal 507a to the address generator 501a.

25 The address generator 501a commands the data storage section 20 to read the bit stream 160 starting from the set read address 506a. The read address and a read instruction of the bit stream 160 are output to the data storage section 20 via the address selection circuit 502 as the address 550.

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The data signal 560 is transmitted from the data storage section 20 based on the read address and the read instruction of the bit stream 160. The data signal 560 is



stored in the FIFO memory 503a. When taking the address of the data storage section 20 indicated by the read address 506a as an initial value, the data signal 560 is a signal representing the data stored in the addresses corresponding to the initial value and subsequent values. When a predetermined amount of the data signal 560 is stored in the FIFO memory 503a, the stored data signal 560 is output to the decoding section 40 as the data signal 561. The data signal 561 is substantially the same as the data signal 560. Thus, the operation of the normal reproduction mode is executed.

In the case where the operation mode is the double speed reproduction mode or the freeze reproduction mode, the operation of the read control section 30 is similar to the operation of the read control section 30 in the normal operation mode up to a point where the data signal 560 is transmitted from the data storage section 20. That is, unlike the normal reproduction mode, the double speed reproduction mode and the freeze reproduction mode use the address generator 501b, instead of the address generator 501a, and the read address 506b and the read starting signal 507b, instead of the read address 506a and the read starting signal 507a, respectively.

The data signal 560 transmitted from the data storage section 20 is stored in the FIFO memory 503b. When taking the address of the data storage section 20 indicated by the read address 506b as an initial value, the data signal 560 is a signal representing the data stored in the addresses corresponding to the initial value and subsequent values.

The data signal 560 stored in the FIFO memory 503b is read by the controller 500. The data signal 560 is the bit stream 160 and includes at least one PES packet 164. (In Figure 7, the PES packets are indicated with reference numerals 164a-164d.) The controller 500 reads the data length of the access unit 151a by analyzing the PES packet 164 and referring to the packet\_length value included in the PES header 141 of the PES packet 164. The controller 500 outputs addresses of every other PES packet 164 (for example, 164a and 164c in Figure 7) for the double speed reproduction mode, or repeatedly outputs the address of one PES packet 164 (for example, 164a in Figure 7) for the freeze reproduction mode, to the address generator 501b as the read address 506b based on the data length of the read access unit 151a. In other words, the process is performed to skip every other PES packet 164 for the double speed reproduction mode, and to read the same PES packet 164 repeatedly for the freeze reproduction mode. Then, the data signal 560 of the address corresponding to the read address 506b and subsequent addresses is read from the data storage section 20 and stored in the FIFO memory 503a. The data signal 560 stored in the FIFO memory 503a is output to the decoding section 40 when the signal reaches a predetermined level.

According to the double speed reproduction operation of the read control section 30 described above, by referring only to the packet\_length value, a skip operation of the PES packets 164 (for example, 164b and 164d in Figure 7) can be implemented. Therefore, a smooth, high-speed reproduction can be implemented.

According to the freeze reproduction operation of

the read control section 30 described above, at least one of the plurality of PES packets 164 generated to include the data corresponding to the access unit is repeatedly decoded. Unlike the case of a conventional device, according to the present invention, the data which has been decoded is not repeatedly displayed, so that a buffer memory for storing the data which has been decoded is not needed.

It is assumed that the controller 500 again outputs the read address to the address generator 501b based on the data length of the read access unit 151a. However, the controller 500 may directly read the corresponding PES packet 164 stored in the FIFO memory 503b based on the data length of the read access unit 151a. In this case, the controller 500 outputs a signal indicating which address in the FIFO memory 503b of the PES packet 164 to be read to the FIFO memory 503b. The FIFO memory 503b which has received the signal indicating the address outputs the data signal 561 including the corresponding PES packets 164 of the address and subsequent addresses to the decoding section 40. This structure is particularly useful for the freeze reproduction operation where one PES packet 164 is repeatedly reproduced.

In the case where the control signal 362 indicates a "triple speed reproduction mode", triple speed reproduction can be implemented by skipping PES packets corresponding to two access units in series and then reproducing PES packets corresponding to one access unit by an operation similar to the operation described above.

Moreover, there may be a case where the control read section 30 cannot perform a skip operation due to a coding

5 scheme, which is based on a forward motion prediction and backward motion prediction which are specific to the MPEG standard. For example, in an image including "I/P/B/B/P/B/B/P-----", only B can be skipped. This operation can easily be implemented by checking a picture coding type following the picture start code 162a.

10 There is no particular limitation on the operation of skipping the PES packets for the audio data.

15 The FIFO memories 503a and 503b are used in this embodiment for an efficient use of a signal line between the read control section 30 and the decoding section 40. This is due to a fact that a signal is transmitted relatively slowly between the read control section 30 and the decoding section 40 while a signal can be transmitted quickly between the read control section 30 and the data storage section 20. By providing the FIFO memories 503a and 503b and starting the transmission when the stored data reaches a predetermined amount, a signal line having a relatively slow transmission speed can be efficiently used.

#### INDUSTRIAL APPLICABILITY

25 According to the present invention, a new packet including data corresponding to an access unit is generated by a packet regeneration section. The new packet includes information indicating a data length corresponding to the access unit. A leading portion of an access unit is easily specified by referring to the information indicating the data length corresponding to the access unit. Unlike the case of a conventional device, according to the present invention, it is not necessary to search a data portion of

30

the packet in order to specify an access unit. Thus, a fast skip reproduction operation can be implemented.

5       According to the present invention, a freeze reproduction operation is implemented by repeatedly decoding at least one of a plurality of new packets generated to include data corresponding to the access unit. Thus, a buffer memory to store the data which has been decoded is not necessary. As a result, system cost is reduced.

10

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## CLAIMS

1. A decoding device for decoding a bit stream including a plurality of packets, in which data corresponding to an access unit includes a first data portion and a second data portion, the decoding device comprising:

5 a packet regeneration section for receiving a first packet and a second packet following the first packet, and when the first packet includes the first data portion and the second packet includes the second data portion, producing a new packet including the data corresponding to the access unit by combining the first data portion and the second data portion; and

10 a decoding section for decoding the data corresponding to the access unit,

wherein the new packet includes information indicating a length of the data corresponding to the access unit.

2. A decoding device according to claim 1, wherein the new packet further includes information indicating a presentation time stamp.

3. A decoding device according to claim 1, wherein the packet regeneration section generates a plurality of new packets, the decoding device further comprising:

25 a storage section for storing the plurality of new packets generated by the packet regeneration section; and

a read control section for controlling a reading operation of the plurality of new packets from the storage section so as to skip at least one of the plurality of new packets by using the information indicating the length of the data corresponding to the access unit.

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4. A decoding device according to claim 1, wherein the packet regeneration section generates a plurality of new packets, the decoding device further comprising:

- 5       a storage section for storing the plurality of new packets generated by the packet regeneration section; and  
      a read control section for controlling a reading operation of the plurality of new packets from the storage section so as to repeatedly read at least one of the plurality of new packets by using the information indicating the length  
10      of the data corresponding to the access unit.

5. A decoding method for decoding a bit stream including a plurality of packets, in which data corresponding to an access unit includes a first data portion and a second data  
15      portion, the decoding method comprising the steps of:

- receiving a first packet and a second packet following the first packet, and when the first packet includes the first data portion and the second packet includes the second data portion, producing a new packet  
20      including the data corresponding to the access unit by combining the first data portion and the second data portion; and

- decoding the data corresponding to the access unit, wherein the new packet includes information indi-  
25      cating a length of the data corresponding to the access unit.

## ABSTRACT

5 A decoding device 1 decodes a bit stream including  
a plurality of packets. Data corresponding to an access unit  
includes a first data portion 150a-1 and a second data  
portion 150a-2. The decoding device 1 includes a packet  
regeneration section 10 for receiving a first packet 130  
and a second packet 130 following the first packet 130, and  
when the first packet 130 includes the first data por-  
tion 150a-1 and the second packet 130 includes the second  
data portion 150a-2, producing a new packet 164 including  
the data corresponding to the access unit by combining the  
first data portion 150a-1 and the second data portion 150a-2.  
The decoding device 1 also includes a decoding section 40  
15 for decoding the data corresponding to the access unit. The  
new packet 164 includes information indicating a length of  
the data corresponding to the access unit.

F03020-2474260



FIG. 1

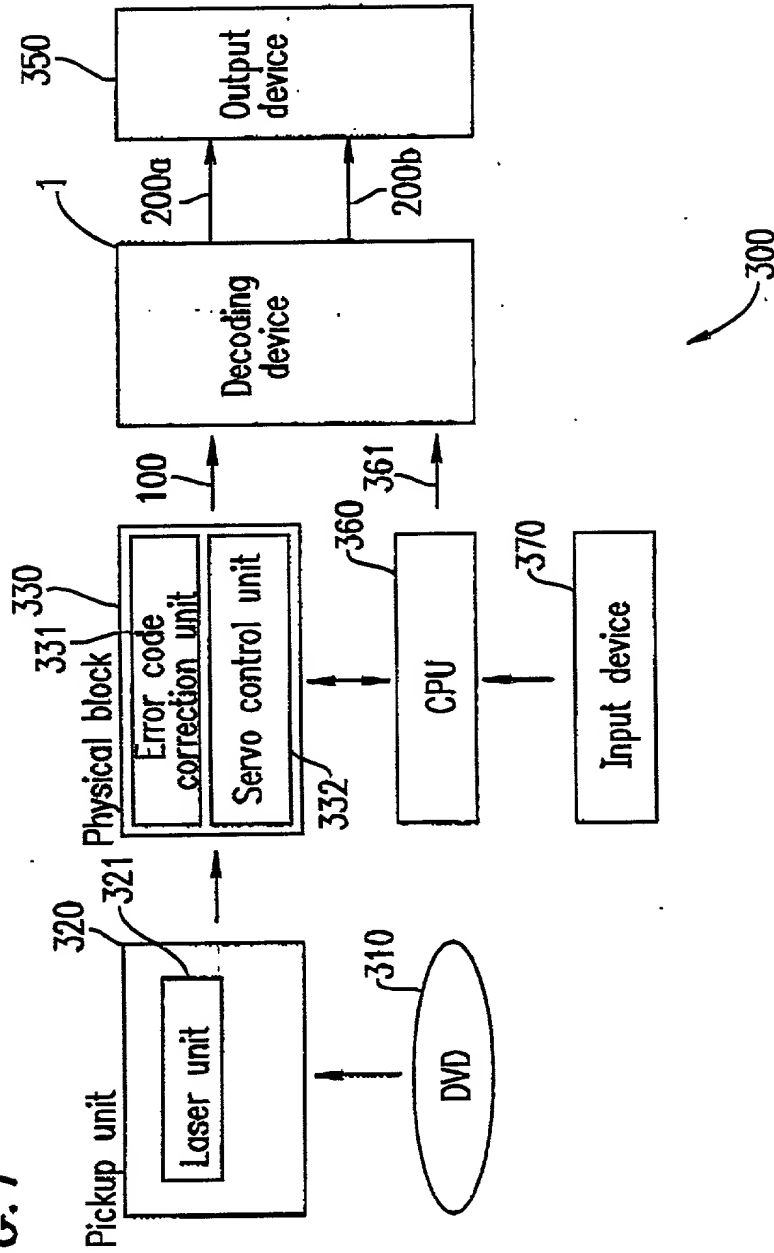


FIG. 2A

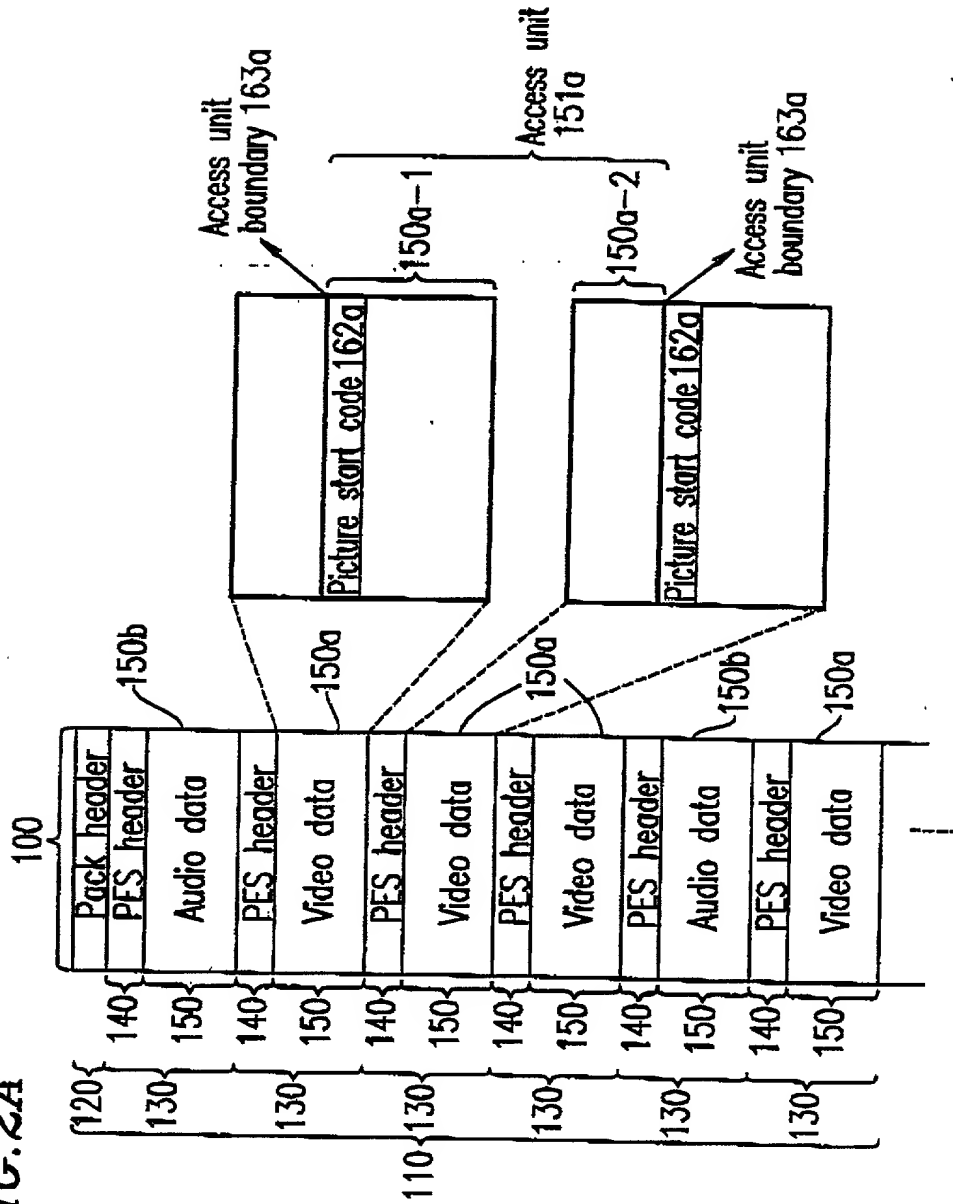


FIG. 2B

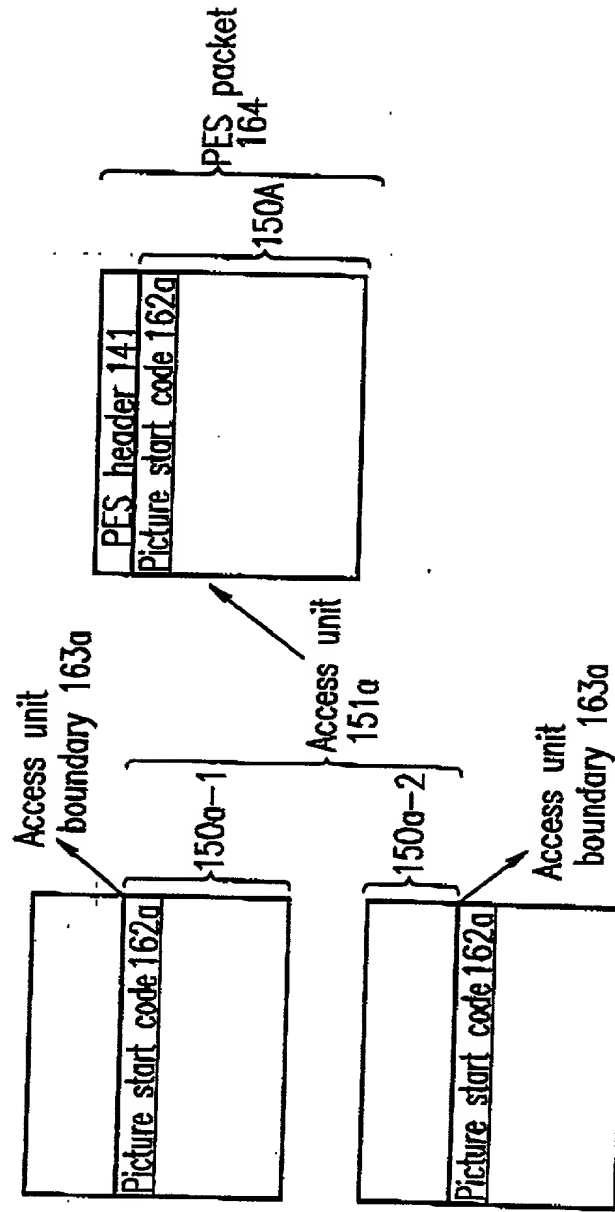
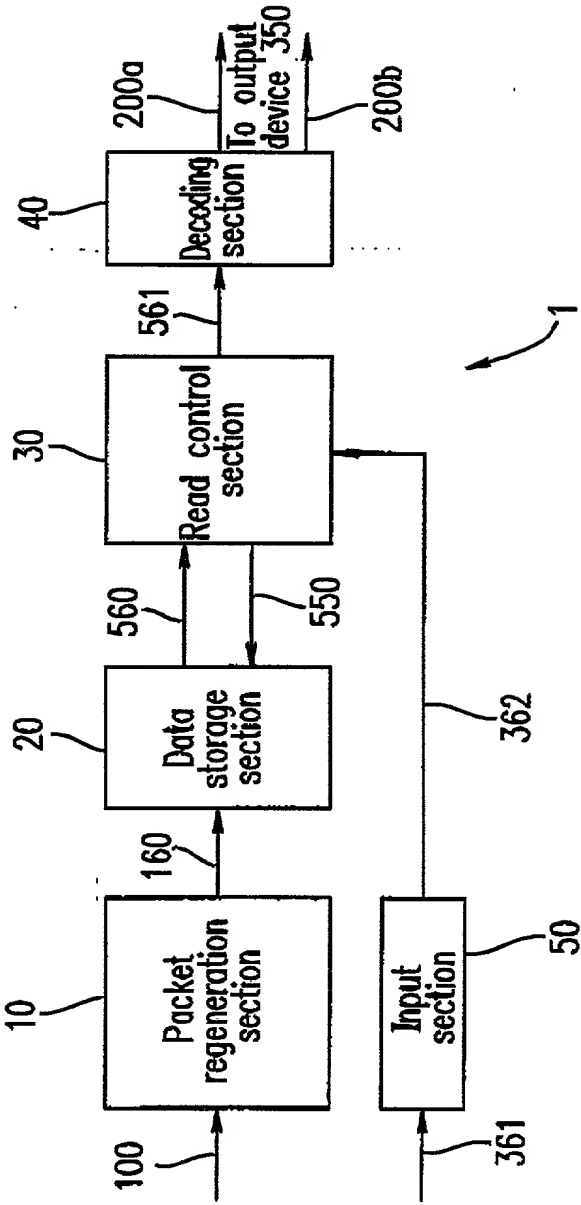
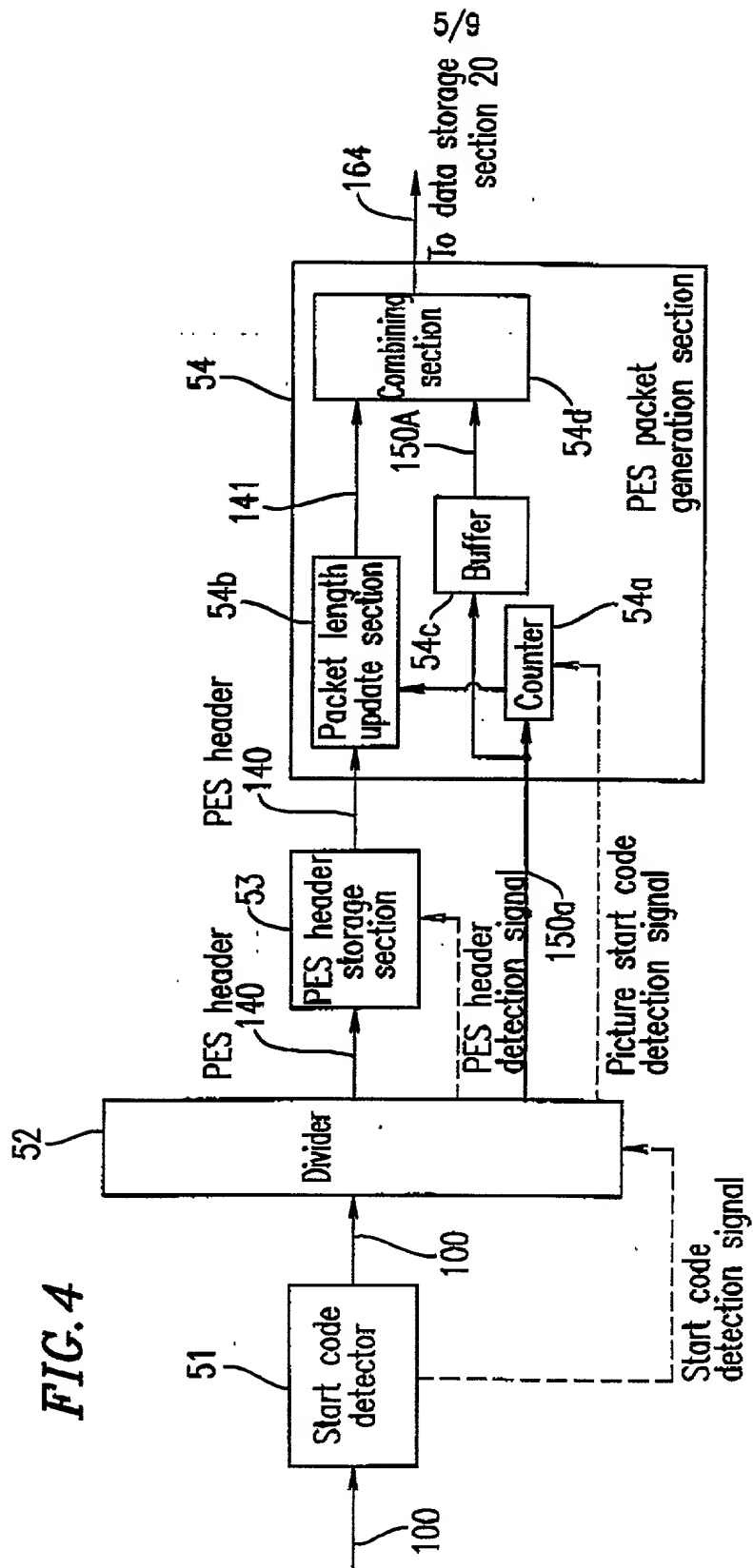


FIG. 3

FIG. 3





10

FIG. 5

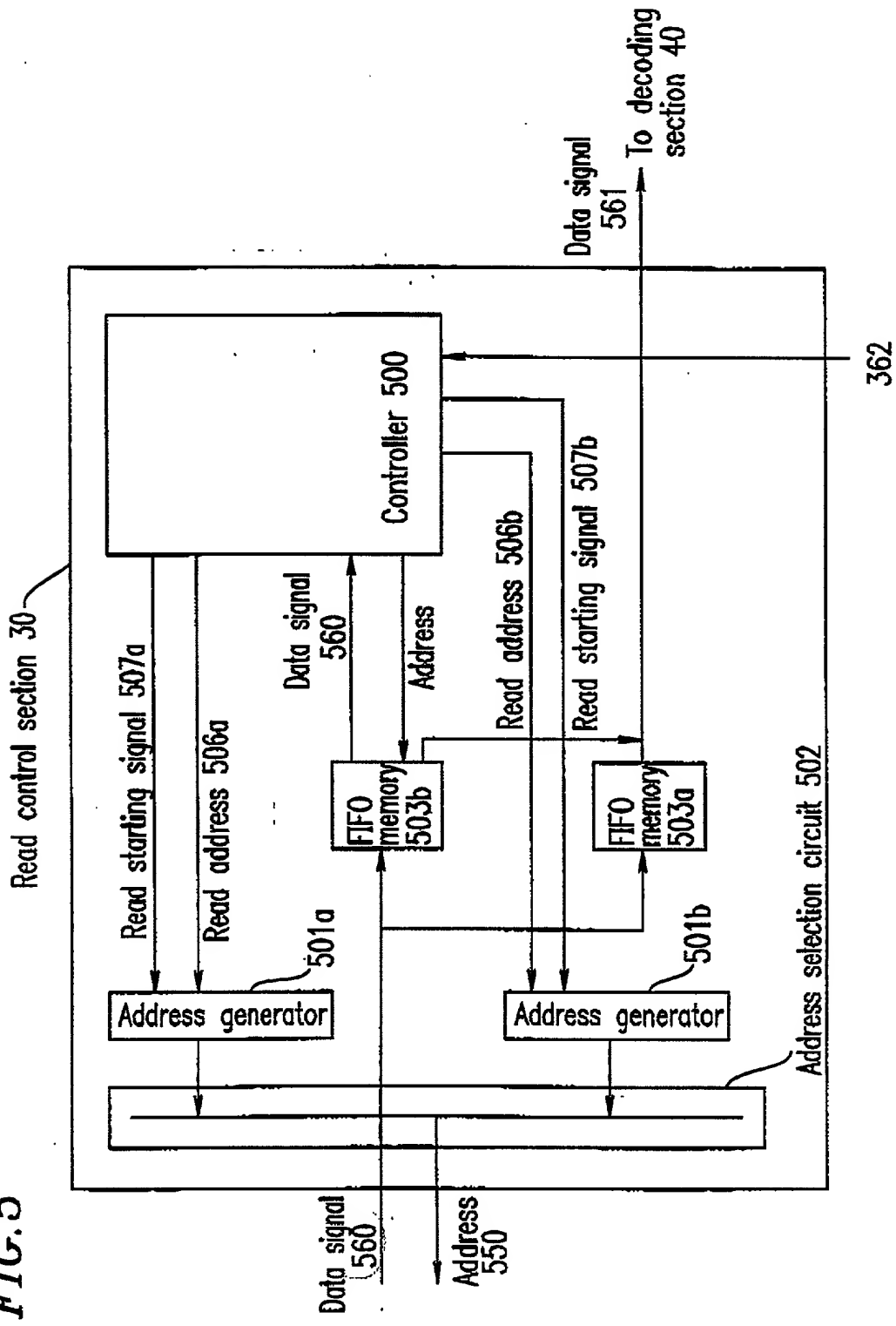


FIG. 6A

Syntax of pack header 120

Pack() {

    pack\_start\_code

    '0010'

    system\_clock\_reference[32:30]

    marker\_bit

    system\_clock\_reference[29:15]

    marker\_bit

    system\_clock\_reference[14:0]

    marker\_bit

    marker\_bit

    mux\_rate

    marker\_bit

5

Example of bit array of pack header 120

```

0000 0000 0000 0000 0000 0000 0001 1011 1010
'0010'
000
1
0000 0000 0000 0000 0000 0000
1
0000 0000 0000 0000 0000 0000
1
0000 0000 0000 0000 0000 0000
1
0000 0000 0000 0000 0000 0000 01
1
    
```

FIG. 6B

Syntax of PES header 140

Packet() {

    pack\_start\_code\_prefix

    stream\_id

    packet\_length

    for (i=0; i<N; i++) {  
        packet\_data\_byte

Example of bit array of PES header 140

0000 0000 0000 0000 0000 0001

1110 0000

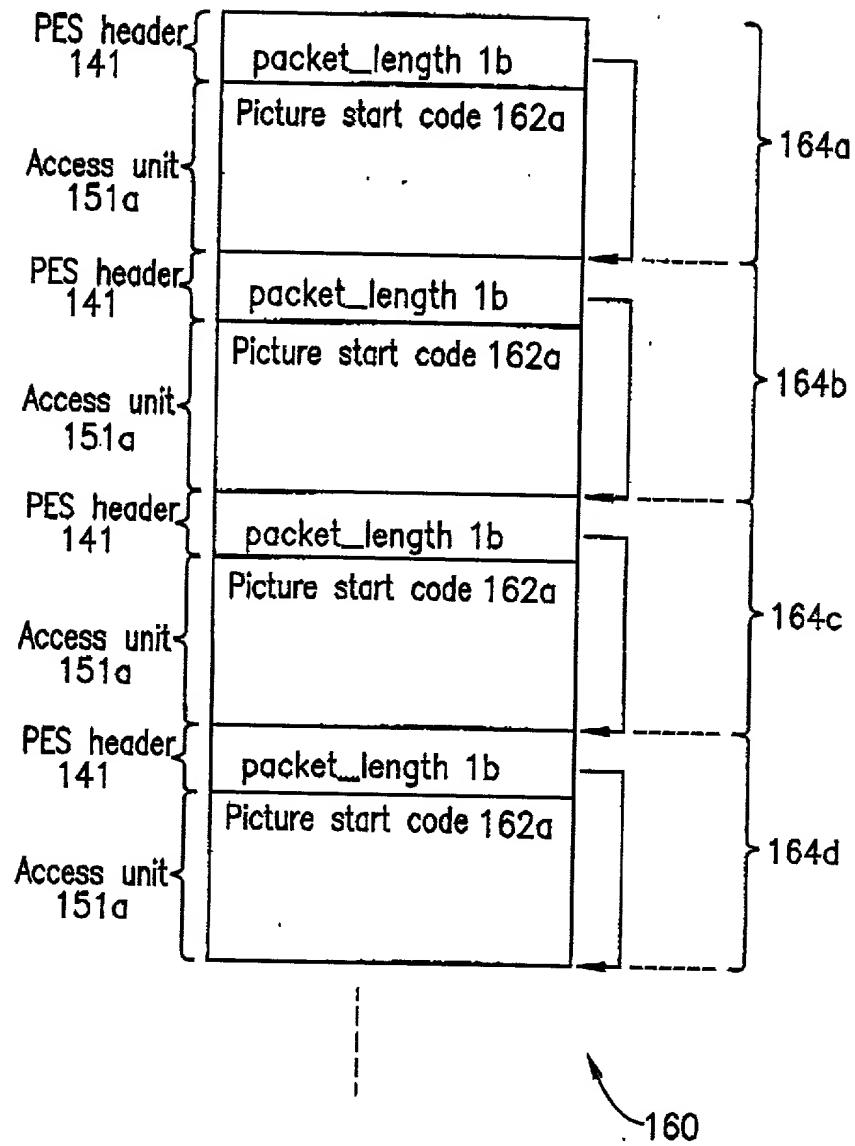
0000 0000 1111 1111

5

5

}



**FIG. 7**

PATENT (US)

Attorney Docket No. YAMAP0749US

COMBINED DECLARATION AND POWER OF ATTORNEY  
(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Title: DECODING DEVICE AND DECODING METHOD

the specification of which

- (a)    is attached hereto.  
 (b) x was filed on January 5, 2001 as X Serial No. 09 / 743,143 or    Express Mail No.                     , as Serial No. not yet known, and was amended on                      (if applicable).  
 (c) x was described and claimed in PCT International Application No. PCT/JP99/03766 filed on July 13, 1999 and amended under PCT Article 34 on                      (if any).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations §1.56(a).

PRIORITY CLAIM

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

- (d)    no such application have been filed.  
 (e) x such applications have been filed as follows.

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COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 USC 119
<u>Japan</u>	<u>10-200996</u>	<u>15/07/98</u>	<u>x</u> Yes <u>  </u> No

ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS  
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POWER OF ATTORNEY

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (List name and registration number)

3 Armand P. Boisselle, Reg. No. 22,381; Neil A. DuChes, Reg. No. 26,725; Mark D. Saralino, Reg. No. 34,243

The undersigned to this declaration and power of attorney hereby authorizes the U.S. attorney(s) named herein to accept and follow instruction from

Name(s) of authorized representation(s) Shusaku Yamamoto Patent Law Office

Address Fifteenth Floor, Crystal Tower, 1-2-27 Shiomi, Chuo-Ku, Osaka 540, Japan

as to any actions to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney(s) and the undersigned. In the event of a change in the person(s) from whom instructions may be taken, the U.S. attorney(s) will be so notified by the undersigned.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued therein.

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Date \_\_\_\_\_ Country of Citizenship \_\_\_\_\_

Residence \_\_\_\_\_

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